REMARKS/ARGUMENTS

Claims 1-31 were pending in the Application. By this amendment, claims 1, 15, 16, 17 and 18 are being amended, claims 24-31 are being cancelled, and new claims 32-35 are being added, to advance the prosecution of the application. No new matter is involved.

In the Office Action of July 27, 2005, all of the claims are rejected on various combinations of U.S. Patent 5,537,650 of West et al., U.S. Patent 5,552,836 of Nobuoka, U.S. Patent 4,544,912 of Iwamoto et al., U.S. Patent 6,087,816 of Volk, U.S. Patent 4,347,474 of Brooks et al., U.S. Patent 6,323,851 of Nakanishi, U.S. Patent 5,155,840 of Niijima and U.S. Patent 6,078,319 of Bril et al. These rejections are respectfully traversed.

The Office Action rejects claims 1 and 15-23 on the combination of West et al. '650 and Nobuoka '836, and various other claims on the combination of those two references together with some of the various other references. However, neither West nor Nobuoka describes or suggests reduction of the supply voltage to the digital-to-analog converter circuit during the "display period". As Applicants have previously explained, West performs the processing during the blanking period, i.e. the non-display period. In addition, West sets the supply voltage to "0", rather than reducing the supply voltage to a voltage which allows display. More specifically, in West no power is supplied to the D/A converter circuit during this period, and it is therefore impossible for the D/A converter circuit to operate in this state. Stated another way, with the supply voltage being 0, an analog signal cannot be output and data necessary for display cannot be obtained. It is because no display is performed that in West, the supply voltage of the D/A converter circuit is set to 0 only during the "blanking period" which is a non-display period.

Similarly, in Nobuoka, the power supply is turned OFF during the vertical blanking period, and not the "display period". Moreover, the Office Action seems to regard the digital-to-analog converter circuit for reducing the supply voltage to be supplied in the present invention, and the analog-to-digital converter circuit of Nobuoka as equivalent elements. However, an analog-to-digital (A/D) converter circuit and a digital-to-analog (D/A) converter circuit differ not only simply in whether they change an analog input signal or a digital input signal and produce a digital output signal or an analog output signal, but also in that they have a completely different influence on how they reduce the supply voltage in the converter circuits, as explained hereafter.

In the first place, in a circuit for converting an analog signal into a digital signal as described in Nobuoka, with a reduction of the supply voltage, the sampling voltage of the analog signal changes with respect to the reference voltage which is used for digitization. With this structure, it is not possible to convert an analog signal which is supplied into a corresponding digital signal correctly. Also, in the processing circuit for a digital signal, as each voltage level in accordance with "1" and "0" of a digital signal changes, information "1" or "0" cannot be transmitted correctly. In addition, even when "0" is transmitted incorrectly in place of "1", this is only treated as incorrect data, and a reduction in the power consumption in a digital processing circuit cannot be normally achieved.

As described above, in Nobuoka, the A/D converter circuit substantially performs no conversion operation if the supply voltage is reduced. This is exactly the reason why the power supply is placed in an off state "only during the vertical blanking period". Accordingly, as in West, Nobuoka is also completely blind to the concept that the supply voltage is reduced "during the display operation" to thereby reduce the power consumption, while allowing the A/D converter circuit to operate.

Further, with regard to the supply voltage supplied to the A/D converter circuit 12, the Office Action states that Nobuoka reduces the supply voltage to a "non-zero voltage". However, nowhere does the reference disclose supply of a non-zero voltage. Rather, Nobuoka only describes that "the A/D converter 12 and the line memories 14 and 16" are "placed in a power supply off state (or a low power consumption state)". In addition, Nobuoka includes no specific suggestion regarding the state in which the A/D converter is placed to reduce the power consumption. Further, it is common knowledge of one of ordinary skill in the art that a correct digital signal cannot be obtained with a simple reduction of the supply voltage, as described above. It is for this reason that, in Nobuoka, the A/D converter is placed in "a power supply off state (or a low power consumption state)" only during the vertical blanking period, which is a "non-display period".

Consequently, with a combination of West and Nobuoka, even a motivation to obtain the invention defined in claims 1, 15, 16, and so forth, in which the voltage supplied to a digital-to-analog converter circuit for converting digital display data into analog display data is reduced to a voltage which allows the D/A converter circuit to perform a conversion operation during the "normal display operation period" cannot be obtained.

Bril discloses that the operation voltage to a video controller IC is reduced from 5V to 3.3V, and that when a voltage of 3.3V is supplied, the operation frequency is reduced and display with a low resolution can be achieved. Bril, however, is completely blind to what should be done to reduce the power consumption while maintaining the resolution and the display quality itself.

At the vary least, Bril nowhere describes or anticipates a D/A converter circuit and an analog processing circuit as built-in circuits of the controller, nor selective reduction of a voltage supplied to these circuits. The present invention

achieves the reduction in the power consumption as described above by reducing the voltage supplied to these circuits. With a simple reduction in the frequency, it is not possible to reduce the power consumption of a circuit which processes these analog signals, and as is clear from Bril, excessive reduction in the frequency makes display impossible. Further, according to the present invention, by reducing the voltage supplied to the digital-to-analog converter circuit, the amplitude of an analog display signal to be output is reduced. Because it is an analog signal, it is possible to reduce the power consumption with the number of display tones and the resolution in the display section being maintained and not decreased. Bril, on the other hand, has no disclosure concerning such a method of reducing the power consumption without deteriorating the display quality, with the display being maintained.

Accordingly, even when the description of Bril is considered in combination with West and Nobuoka, the present invention cannot be obtained.

As amended herein, claim 1 defines driving apparatus for a display device which includes a driving circuit and a power supply circuit, with the power supply circuit reducing the supply voltage supplied to a digital-to-analog converter circuit and to an analog signal processing circuit from the supply voltage during the normal operation to a voltage which still allows the digital-to-analog converter circuit and the analog signal processing circuit to operate, when a predetermined power save is instructed. As amended, claim 1 further defines the driving apparatus in terms of a period in which the power save is instructed and the supply voltage is reduced includes a period in which display data is written to the display region and a display is realized. Further, as amended, the driving apparatus defined in terms of during a period in which the power save is instructed and the supply voltage is reduced, the digital-to-analog converter circuit outputs an analog

signal corresponding to a digital signal. In addition, the digital-to-analog converter circuit is defined as converting a digital "display" signal to an analog "display" signal, and the analog signal processing circuit is defined as processing an analog "display" signal.

Claims 15, 16, 17, and 18 are being amended in similar fashion. Accordingly, such claims are submitted to clearly distinguish patentably over the cited art. As described above, none of the references describe the structure for performing display and also reducing the power consumption without deterioration of display quality, or a power supply circuit corresponding to such a structure.

Similar comments apply to new claims 32-35. Claims 32 and 33 depend from and further define claim 1. Claim 34 which is an independent claim defines a display device as comprising a driving apparatus defined in terms the same as those of claim 1. In addition, the display device of claim 34 is defined in terms of the display sector providing a display in response to a signal provided by the driving apparatus, and the display device being switchable between a normal display mode and a power save mode. Claim 35 depends from and further defines claim 34 in terms of additional details.

Similarly, claims 2-14 depend directly or indirectly from and contain all of the limitations of claim 1, so that such claims are also submitted to clearly distinguish patentably over the cited art.

In conclusion, claims 1-23 and 32-35 are submitted to clearly distinguish patentably over the cited art for the reasons set forth above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los

Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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